In the Claims:

Please amend claims 1, 8 and 26.

The claims are as follows:

1. (Currently Amended) A ~~software~~ system for verifying an integrated circuit design, said system comprising:

an external memory mapped test device having a switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding virtual I/O buses;

a virtual memory bus connecting said I/O controller and said switch; and

wherein said external memory mapped test device is a software module, said I/O cores and said I/O controller are software descriptions of said integrated circuit design and said external memory mapped test device software module, said I/O cores and said I/O controller are executable by a test operating system.

2. (Original) The system of claim 1, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models.

3. (Previously Presented) The system of claim 1, wherein said external memory mapped test device further includes an address register.

4. (Previously Presented) The system of claim 1 wherein said integrated circuit design further includes an embedded processor.

5. (Previously Presented) The system of claim 2, wherein each said external memory mapped test device module further includes an address register.

6. (Previously Presented) The system of claim 2, wherein said integrated circuit design further includes an embedded processor.

7. (Original) The system of claim 1, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models and further including an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design.

8. (Previously Presented) A ~~software~~ method for verifying an integrated circuit design, the method comprising:

providing an external memory mapped test device software module having a switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding virtual I/O buses;

providing a virtual memory bus connecting said I/O controller and said switch;

programming connections of said external memory mapped test device and connections of a general purpose I/O core to said I/O models;

wherein said I/O cores, said general purpose I/O core and said I/O controller are software descriptions of said integrated circuit design; and

simulating said integrated circuit design by running a test case with said programmed connections.

9. (Original) The method of claim 8, further including:

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models.

10. (Previously Presented) The method of claim 8, further including:

providing said external memory mapped test device with an address register ~~for~~; and setting said switch and controlling said I/O driver models using address information programmed into said address register.

11. (Previously Presented) The method of claim 8 further including:

providing an embedded processor in said integrated circuit design, said embedded processor running said test operating system controlling said software.

12. (Previously Presented) The method of claim 9, further including:

providing each external memory mapped test device with an address register; and

setting each portion of said switch and controlling each I/O driver model using address information programmed into said address register.

13. (Previously Presented) The method of claim 9 , further including:

providing said integrated circuit design with an embedded processor running said test case on said embedded processor.

14. (Previously Presented) A method for verifying an integrated circuit design comprising:

providing an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design;

providing an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models;

providing a bus for transferring signals between said I/O controller and said switch;

providing a test operating system for controlling said switch;

simulating said integrated circuit design by running a test case on said test operating system;

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models: and

providing an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design.

15. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for verifying an integrated circuit design, said method steps comprising:

providing an external memory mapped test device software module having a switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding virtual I/O buses;

providing a virtual memory bus connecting said I/O controller and said switch;

programming connections of said external memory mapped test device and connections of a general purpose I/O core to said I/O models;

wherein said I/O cores, said general purpose I/O core and said I/O controller are software descriptions of said integrated circuit design; and

simulating said integrated circuit design by running a test case with said programmed connections.

16. (Original) The program storage device of claim 15, said method steps further including:

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models.

17. (Previously Presented) The program storage device of claim 15, said method steps further including:

providing said external memory mapped test device with an address register; and setting said switch and controlling said I/O driver models using address information programmed into said address register.

18. (Previously Presented) The program storage device of claim 15, said method steps further including:

providing an embedded processor in said integrated circuit design, said embedded processor running said test operating system controlling said software.

19. (Previously Presented) The program storage device of claim 16, said method steps further including:

providing each external memory mapped test device with an address register; and setting each portion of said switch and controlling each I/O driver model using address information programmed into said address register.

20. (Previously Presented) The program storage device of claim 16, said method steps further including:

providing said integrated circuit design with an embedded processor running said test case on said embedded processor.

21. (Previously Presented) The system of claim 1, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores, universal asynchronous receiver transmitter cores, serial cores, and general purpose I/O cores.

22. (Previously Presented) The system of claim 1, wherein said integrated circuit design further includes an embedded processor core, a memory controller core and a direct memory access core.

23. (Previously Presented) The system of claim 22, further including a direct memory access core model of said a direct memory access core.

[[22]] 24. (Previously Presented) The method of claim 8, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores, universal asynchronous receiver transmitter cores and serial cores.

25. (Previously Presented) The method of claim 8, wherein said integrated circuit design includes an embedded processor core, a memory controller core and a direct memory access core.

26. (Currently Amended) The method of claim [[26]] 24, wherein said integrated circuit design includes a direct memory access core model of said a direct memory access core.

27. (Previously Presented) The program storage device of claim 15, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores, universal asynchronous receiver transmitter cores and serial cores.

28. (Previously Presented) The program storage device claim 15, wherein said integrated circuit design includes an embedded processor core, a memory controller core and a direct memory access core.

29. (Previously Presented) The program storage device of claim 27, wherein said integrated circuit design includes a direct memory access core model of said a direct memory access core.

30. (Previously Presented) The method of claim 8, further including:

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models: and

connecting an additional external memory mapped test device module directly to one or more additional I/O driver models and directly connecting each additional I/O driver model to an additional I/O core, each additional I/O core part of said integrated circuit design